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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/713,446	11/15/2000	VENKAT V EASWAR	TI-22423	3256

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EXAMINER	
PENDERGRASS, KYLE M	
ART UNIT	**PAPER NUMBER**
2624	

DATE MAILED: 07/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/713,446	EASWAR, VENKAT V	
	Examiner	Art Unit	
	Kyle M Pendergrass	2624	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 15 November 2000 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Applicant discloses Figures 1-9 as prior art. It is requested that the applicant include references to this prior art. It appears that Balmer et al., (US 5,606,677) discloses similar art with the exception of the print buffer and print engine of Figure 1.

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Claim 1 line 10-15 states 3 sequential steps of addition, saturation and truncation, however the specification discloses only a simultaneous operation of the three steps (pages 68-70). For this reason, applicant's sequential process steps of addition, saturation, and truncation are not understood and are not considered to be enabling.

3. Claims 1-8 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. There is a lack of written description for truncation

of saturated components in the Specification (pages 69 &70). Claim 1 describes truncation of saturated sum data words, however the Specification only discusses the truncation to be preformed when saturation does not occur. For these reasons, how and when applicant's truncation occurs is not understood. For this reason applicant's truncation process is not considered to be enabling.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ulichney (US 5,912,745) and Balmer et al (US 5,606,677). Ulichney teaches defining a dither value for each pixel of a matrix in column 2, lines 52-54. Ulichney also teaches the packing of plural pixel values and corresponding plural dither values in column 7, lines 37-43. The dithering system discloses translating input pixels containing plurality of chrominance and luminance values and having input level representation into output level representations for code words. The dithering system also discloses corresponding dither values that are stored in a matrix memory for later use. Ulichney further discloses a saturated coded sum word in column 10, Equation Set II. Saturation occurs when the weighted value is added to the pixel value for each element in the

pattern array, which has its own particular value. Referring now to Figure 8, Ulichney discloses truncation of the summed code word in column 12, lines 11-13. As described, a predetermined number of minority bits are removed, forming the output image word.

However, Ulichney does not teach adding the coded pixel values and corresponding coded dither values in an arithmetic logic unit (ALU) selectively splittable, but does indicate that the values are added by an adder in column 8 lines 29-31.

Figure 7 disclosed by Balmer et al (US 5,606,677) teaches a splittable ALU, capable of adding coded pixel values and corresponding coded dither values. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the ALU instead of the adder because of the added versatility provided by its splittable attribute. The attribute would have provided greater operational function for the system disclosed by Ulichney.

Regarding Claim 2, the claim rejection of claim 1 meets the subject matter of claim. Ulichney teaches saturation of pixel values (column 10, Equation Set II) which provides equivalent saturation as claimed by the applicant, although Ulichney accomplishes saturation under a substitute saturation technique and an alternative methodology than is suggested by the applicant.

However, Ulichney also does not teach saving a carry out in a multiple flags data word. Figure 7 (and its description in column 23, lines 27-30) also discloses saving a carry out in a multiple flags data word. Storing the carry out is a proven method for control masks that would be used in operations.

Regarding Claim 3, the claim rejection of claim 1 meets the subject matter of claim 3. Claim 3 calls for truncating, that is, removing a predetermined number of bits. In column 12 lines 11-15, Ulichney discloses pixel reduction by removing minority bits.

Regarding Claim 4, the claim rejection of claim 1 meets the subject matter of claim 4. Ulichney teaches, in column 6, lines 26-28, that input value representation in fixed point format is well known. It would be obvious to one of ordinary skill that pixel representation can be accomplished using bits format other than that of Ulichney, depending on the level of detail needed.

Regarding Claim 5, the claim rejection of claim 1 meets the subject matter of claim 5. Ulichney teaches the step of quantizing the output image word into threshold ranges in column 2, lines 58-60.

6. Claims 6, 7 & 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ulichney (US 5,912,745), Balmer et al (US 5,606,677), and Taggart (US 5,687,087).

Regarding claim 6, Ulichney teaches defining a dither value for each pixel of a matrix (column 2, lines 52-54), and packing of plural pixel values and corresponding plural dither values (column 7, lines 37-43). The dithering system discloses translating input pixels containing plurality of chrominance and luminance values and having input level representation into output level representations for code words. The dithering system also discloses corresponding dither values that are stored in a matrix memory for later use. Ulichney further discloses a saturated coded sum word in column 10, Equation Set II. Saturation occurs when the weighted value is added to the pixel value

for each element in the pattern array, which has its own particular value. Referring now to Figure 8, Ulichney discloses truncation of the summed code word in column 12, lines 11-13. As described, a predetermined number of minority bits are removed, forming the output image word.

However, Ulichney does not teach adding the coded pixel values and corresponding coded dither values in an arithmetic logic unit (ALU) selectively splittable, but does indicate that the values are added by an adder in column 8 lines 29-31. Ulichney also does not disclose a programmable data processor connected to a transceiver, memory and print engine.

Figure 7 disclosed by Balmer et al (US 5,606,677) teaches a splittable ALU, capable of adding coded pixel values and corresponding coded dither values. Figure 1 disclosed by Balmer et al. discloses an image forming device comprising a transceiver (16) adapted for bidirectional communication with a communications channel; a memory (9); and a programmable data processor (100) connected to said transceiver, said memory and a video display (8). Balmer et al., teaches a programmable data processor (100) programmed to: 1) receive video display data. However, Balmer et al., does not teach a print engine. Taggart teaches a printer (24) connected to a video display (12).

Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the ALU instead of the adder because of the added versatility provided by its splittable attribute. The attribute would have provided greater operational function for the system disclosed by Ulichney. It would have been obvious to one of ordinary skill in the art at the time the invention was made to have

used the processor/video display of Balmer et al., with the dithering system of Ulichney because the video display of Balmer et al., would have allowed the homogeneous and visually pleasing output image described by Ulichney in column 5, lines 5-6 to be displayed. Furthermore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the printer set-up of Taggart to print the video display of Balmer et al., because Taggart's printer would allow for the image to be formed on a printed page according to received image data and control signals.

Regarding claim 7, the claim rejection of claim 6 meets the subject matter of claim 7. Ulichney teaches all of claim 7, but does not teach a multiple flags register connected to the ALU, or an expand circuit connected to the multiple flags register.

However, Balmer et al., teaches a multiple flags register connected to an arithmetic logic unit receiving and storing a carry out (column 17, lines 57-59). Balmer et al., further teaches an expand circuit connected to a multiple flags register for expanding the multiple flags register in order to form a mask data word (columns 19 and 20, lines 64-65 and 14-16, respectively).

Regarding claim 8, the claim rejection of claim 6 meets the subject matter of claim 8. Ulichney teaches all of claim 8, but does not teach a selectable shifter, a mask generator, and truncation. However, Balmer et al., teaches a shifter (column 18, line 1 and Table 1), and a mask generator having an input and an output (Figure 5 and column 18, line 3).

Conclusion

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Kyle Pendergrass whose telephone number is 703-306-3445.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Primary, David Moore, can be reached at 703-308-7452. The fax number for the organization where this application or proceeding is assigned is 703-308-5397.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DAVID MOORE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2